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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,414	09/12/2003	Fernando Gonzalez	MICRON.079DV1C1	6655
20995	7590 06/07/2004		EXAM	INER
KNOBBE M	ARTENS OLSON &	ABRAHAM, FETSUM		
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FOURTEENTH FLOOR			ART UNIT	PAPER NUMBER
IRVINE, CA	92614		2826	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)
	10/661,414	GONZALEZ ET AL.
Office Action Summary	Examiner	Art Unit
	Fetsum Abraham	2826
The MAILING DATE of this communication Period for Reply	appears on the cover sheet w	ith the correspond nce address
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a  - If NO period for reply is specified above, the maximum statutory per  - Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the meanned patent term adjustment. See 37 CFR 1.704(b).	N. R 1.136(a). In no event, however, may a reply within the statutory minimum of thir riod will apply and will expire SIX (6) MON atute, cause the application to become AE	reply be timely filed  ty (30) days will be considered timely.  ITHS from the mailing date of this communication.  BANDONED (35 U.S.C. § 133).
Status		
1)☐ Responsive to communication(s) filed on 2a)☐ This action is FINAL. 2b)☒ T      3)☐ Since this application is in condition for allocation is accordance with the practice under the practice under the practice.	his action is non-final. wance except for formal mat	• •
Disposition of Claims		
4) ☐ Claim(s) 1-8 is/are pending in the application 4a) Of the above claim(s) is/are without 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-8 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and	drawn from consideration.	
Application Papers		
9) The specification is objected to by the Exam  10) The drawing(s) filed on is/are: a) a  Applicant may not request that any objection to the Replacement drawing sheet(s) including the con  11) The oath or declaration is objected to by the	accepted or b) objected to the drawing(s) be held in abeyare rection is required if the drawing	nce. See 37 CFR 1.85(a). (s) is objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of:  1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the papplication from the International Bur	ents have been received. ents have been received in A priority documents have been reau (PCT Rule 17.2(a)).	application No received in this National Stage
* See the attached detailed Office action for a	list of the certified copies not	received.
Attachment(s)    Notice of References (flux) (PTO-892)   Notice of Parisperson's Patent Drawing Review (PTO-948)   Notice of Disclosure Statement(s) (PTO-1449 or PTO/SB/Paner (Ne/s)/Mail Date	Paper No( (08) 5) Notice of I	Summary (PTO-413) s)/Mail Date nformal Patent Application (PTO-152)
Paper Me(s)/Mail Date	6)	<u> </u>

Application/Control Number: 10/661,414

Art Unit: 2826

## **DETAILED ACTION**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung et al (6,436,771).

The prior art discloses an integrated circuit composed of first and second transistors provided with gate dielectric layers different in thickness whereby the first gate dielectric is composed of a thin nitride layer and an oxide layer on and the second provided with an oxide layer first and an oxynitride layer on top. The structure as can be seen in the front page finally produces a first transistor with thinner gate dielectric layer in the integrated two-transistor system. Further, the first thin nitride layer on the first portion of the semiconducting surface indeed limits the oxidation rate of the semiconductor layer underneath while allowing effecting oxidation on the same region through.

As for claim 3, the second gate dielectric layer is thicker than the composite gate dielectric layer of the first transistor.

As for claim 5, an oxide layer is deposed on the nitride film.

As for claim 6, the overall structure of the prior art conforms to a memory device.

As for claim 8, the first and second transistor areas on the substrate are peripheral to each other.

Art Unit: 2826

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,4,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the same prior art.

As for claims 2,4, although the prior art may not have taught of a silicon oxide or an ONO material in the structure, exchanging a dioxide material for an oxide or ONO material is known in the art since the choices allow a specific design to use appropriate dielectric constant that might assist a specific designer with different capacitances as needed in the specific arrangement.

As for claim 7, transistors and specifically MOSFETs are known logic control elements and thus the overall structure of the prior art conforms to a logic control circuit by broad definition.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

upervisor, Nathan J Flynn can be reached at 571-272-1915.

elsum Abraham//6/1/04